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APPLICATION FOR LETTERS PATENT
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TITLE OF INVENTION: MULTI-LEVEL CONDUCTIVE LINES
WITH REDUCED PITCH

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

MULTI-LEVEL CONDUCTIVE LINES WITH REDUCED PITCH

This application is a continuation-in-part of US Patent Application USSN 09/751,492 (Attorney Docket Number 98E9354US).

FIELD OF THE INVENTION

The present invention relates to integrated circuits and, more particularly, to integrated circuits with multi-level conductive lines with reduced line pitch.

BACKGROUND OF THE INVENTION

In integrated circuits, parallel conductive lines are widely used to interconnect circuit elements. Fig. 1 shows conductive lines 120 formed on a substrate 101, separated by line spaces 135. The width of the line spacing and conductive line is referred to as the "line pitch". A limiting factor to reducing the line pitch is the minimum resolution or feature size (F) of a specific lithographic tool. With the line spacing and line width equal to 1F each, the minimum line pitch is 2F.

One technique for reducing line pitch below 2F is to provide an additional level 165 on which second conductive lines 125 are formed. By staggering the lines between first and second levels 160 and 165, a line pitch

of less than 2F can be achieved. Reducing the line pitch is desirable since it reduces chip size, thus reducing manufacturing costs since more chips can be fabricated on a wafer. However, when the line pitch is reduced, the line capacitance increases due to the larger line-to-line capacitance. Larger line capacitance is undesirable as it increases power consumption. In addition, the larger line capacitance can negatively affect the signal integrity due to coupling noise from neighboring lines, reducing yield.

As evidenced from the foregoing discussion, it is desirable to reduce the line pitch in order to reduce the chip area. In addition, it is desirable to reduce the line-to-line capacitance and the total line capacitance for a given pitch.

SUMMARY OF THE INVENTION

The invention relates to multi-level conductive lines having reduced capacitance for a given pitch. In one embodiment, at least conductive lines on one of the multi-levels comprise non-rectangular shaped cross-sections. The use of non-rectangular shaped conductive lines increases the effective spacing between conductive lines, thus reducing capacitance of conductive lines for a given pitch.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 shows an integrated circuit with conventional multi-level conductive lines;

Fig. 2 shows an integrated circuit with multi-level conductive lines in accordance with one embodiment of the invention;

Figs. 3-5 show multi-level conductive lines in accordance with alternative embodiments of the invention;

Figs. 6-9 show a process for fabricating conductive lines in accordance with one embodiment of the invention; and

Figs. 10-14 show a process for fabricating conductive lines in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 2 shows an integrated circuit having multi-level conductive lines in accordance with one embodiment of the invention. A substrate 101 is provided on which conductive lines 220 and 225 are formed. Typically, the width of a conductive line is limited to about 1F. Line widths of greater than 1F can also be used, as desired. The conductive lines are located on first and second conductive levels 260 and 265 and isolated from each other by a dielectric layer 205. The substrate, for example, comprises a dielectric layer over a

semiconductor substrate having circuit features formed thereon. Contacts are provided to electrically couple the circuit features with the conductive lines. However, for sake of simplification, the contacts and circuit features are not shown.

In accordance with the invention, at least the conductive lines on one of the levels comprise non-rectangular cross-sections. Preferably, conductive lines in the different levels comprise non-rectangular cross-sections. In one embodiment, the non-rectangular conductive lines comprise at least one non-vertical sidewall. The non-vertical sidewall tapers toward the other sidewall. Providing conductive lines having two non-vertical sidewalls are also useful. The sidewalls, for example, converge to form conductive lines with a triangular shaped cross-section. Alternatively, the sidewalls do not converge. In one embodiment, conductive lines with non-rectangular shaped cross sections on the lower level have sidewalls tapering towards each other at the top of the conductive lines. Conductive lines with non-rectangular shaped cross-sections on the upper level have sidewalls tapering towards each other at the bottom of the conductive line.

By providing conductive lines with non-rectangular cross-sections, the effective pitch is greater than the actual pitch. For example, as shown in Fig. 2, the pitch

between the lines on the same level is 2F, 1F for the line width and 1F for the line spacing. However, due to the non-vertical sidewalls, the effective spacing between the conductive lines is greater than 1F. Thus, the use of conductive lines with non-rectangular shaped cross-sections reduces the line-to-line capacitance, resulting in a reduction in coupling noise and power consumption for a given pitch.

In one embodiment, the conductive lines on the different levels comprise first and second non-vertical sidewalls 225 and 226 which converge to form a triangular shaped cross-section. The conductive lines on the lower level have sidewalls which taper toward each other at the top of the conductive lines while the conductive lines on the upper level have sidewalls which taper at the bottom of the conductive lines. As shown, the top and bottom of the conductive lines on the different levels are coplanar. Providing conductive lines with non-rectangular shaped cross sections on different levels can reduce the overall height of the device without increasing the line-to-line capacitance. This is because the effective spacing between the lines on the different levels is greater than the actual line spacing between the different levels. For example, as shown in Fig. 2, the actual distance between the two levels is zero (two levels are contiguous) but the effective distance between

the top of the conductive lines on the lower level and the bottom of the conductive lines on the upper level is about 1F. Alternatively, the distance between the two levels can be increased to reduce the line-to-line capacitance between conductive lines on the different levels as desired.

Fig. 3 shows an alternative embodiment of the invention for reducing capacitance for a given pitch. Conductive lines 320 and 325 are formed in respective first and second levels 260 and 265. The conductive lines comprise a vertical sidewall and a non-vertical sidewall. The non-vertical sidewall tapers toward the vertical sidewall. In one embodiment, sidewalls converge. In one embodiment, adjacent sidewalls of adjacent conductive lines on the different levels have substantially the same angle. Like the embodiment described in Fig. 2, the use non-rectangular shaped cross-sections enables a reduction in the overall height of the device without increasing the line capacitance or line-to-line capacitance.

Fig. 4 shows another embodiment of the invention. The conductive lines 420 and 425 are formed on first and second levels 260 and 265. The conductive lines comprise first and second non-vertical sidewalls which taper toward each other. The sidewalls do not converge. Like the embodiments described in Figs. 2-3, the use non-

rectangular shaped cross-sections enables a reduction in the overall height of the device without increasing the line-to-line capacitance or coupling capacitance between the conductive lines of the different levels.

Fig. 5 shows yet another embodiment an IC with multi-level conductive lines. The conductive lines 520 and 525 are located on first and second levels 260 and 265 on the substrate. Conductive lines on one level have rectangular-shaped cross-sections while the conductive lines on the other level have non-rectangular-shaped cross-sections. In one embodiment, the first conductive lines on the lower level have rectangular-shaped cross-sections while the second conductive lines on the upper level have non-rectangular cross-sections. The second conductive lines, in one embodiment, comprise non-vertical sidewalls which taper toward each other toward the bottom to form triangular-shaped cross-sections. The use of non-rectangular shaped conductive lines in at least one level results in smaller capacitance between the conductive lines of the different levels for a given line pitch than conventional approaches using of rectangular shaped conductive lines.

Figs. 6-11 show a process for forming conductive lines in accordance with one embodiment of the invention. Referring to Fig. 6, a substrate 101 is provided. Above the substrate is deposited a conductive layer 620. The

conductive layer comprises, for example, aluminum, copper, or alloys thereof. Other types of conductive materials can also be used. A mask layer 650, such as resist, is deposited and patterned to selectively expose portions of the conductive layer.

Referring to Fig. 7, the conductive layer is patterned. In one embodiment, the conductive layer is patterned using, for example, an isotropic etch. The isotropic etch comprises, for example, a wet etch. The etch forms conductive lines 220 beneath the resist. In one embodiment, the conductive lines comprise triangular shaped cross-sections. After the conductive lines are formed, the resist is removed.

Referring to Fig. 8, a dielectric layer 205 is deposited over the conductive lines. The dielectric layer comprises, for example, silicon oxide, silicate glass, doped silicate glass, or silicon nitride. The dielectric layer can be planarized as necessary to provide a planar top surface. The use of a self-planarizing dielectric material, such as spin-on-glass, is also useful. In one embodiment, the thickness of the dielectric layer is about twice the thickness of the conductive lines. A mask layer 850 is deposited and patterned, exposing portions of the dielectric layer. In one embodiment, the resist covers the dielectric layer above the conductive lines 220.

In Fig. 9, the dielectric layer is etched using an isotropic etch. The etch forms trenches 977 with non-vertical sidewalls tapering toward each other to form triangular-shaped trenches. After the trenches are formed, the mask layer is removed. Subsequently, a conductive layer (not shown) is deposited over the dielectric layer to fill the trenches. The structure is then polished by, for example, chemical mechanical polishing (CMP) to remove excess conductive material, leaving conductive lines in the trenches. Additional processing is performed to complete the IC.

Figs. 10-14 show a process for forming conductive lines in accordance with another embodiment of the invention. Referring to Fig. 10, a substrate 101 with a dielectric layer 205 deposited thereon is provided. The dielectric layer is patterned, forming trenches 1021. The trenches, in one embodiment, comprise substantially vertical sidewalls. Vertical sideswalls can be obtained by anisotropic etching techniques (e.g., ion milling or reactive ion etching).

Referring to Fig. 11, a conductive layer 1120 is deposited on the dielectric layer. The conductive layer comprises, for example, aluminum, copper, or alloys thereof. Other types of conductive materials can also be used. If necessary, the surface of the conductive layer is planarized to provide a planar top surface.

Referring to Fig. 12, a mask layer 1250, such as resist, is deposited and patterned to expose portions of the conductive layer. In one embodiment, the resist covers the portions of the conductive layer where conductive lines on the second level are to be formed.

Referring to Fig. 13, the conductive layer is patterned. In one embodiment, the conductive layer is patterned using, for example, an isotropic etch. The isotropic etch comprises, for example, a wet etch. Other isotropic etch techniques, are also useful. The etch forms conductive lines 520 in the trenches and conductive lines 525 above the dielectric layer. The conductive lines 525, in one embodiment, comprise non-vertical sidewalls that taper toward each other, forming triangular-shaped cross-sections. In one embodiment, the conductive lines comprise triangular- shaped cross-sections. After the conductive lines are formed, the resist is removed.

Referring to Fig. 14, a dielectric layer 206 is deposited, covering the conductive lines and dielectric layer 205. The dielectric layer comprises, for example, oxide, silicate glass, silicon nitride, or doped silicate glass. The dielectric layer can be planarized as necessary to provide a planar top surface. The use of a self-planarizing dielectric material, such as spin-on-

glass, is also useful. Additional processing is performed to complete the IC.

While the invention has been particularly shown and described with reference to various embodiments, it will be recognized by those skilled in the art that modifications and changes may be made to the present invention without departing from the spirit and scope thereof. The scope of the invention should therefore be determined not with reference to the above description but with reference to the appended claims along with their full scope of equivalents.